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10/766,852	01/30/2004	Roderick A. Barman	P388 0008	3901

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,852	BARMAN ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7,9,12,14-16,18-26 and 29-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,9,12,14-16,18-26 and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 2 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant did not disclose the subject matter "wherein the time measurement for the second bus is taken midway between the first and second time measurements for the first bus" in the original specification. Furthermore, it is not clear from what the midway would be considered relative to [e.g., first, second or global time measurement]. Examiner will take the position that midway is sometime between the first and second time measurements for the first bus in order to apply prior art.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant did not specifically identify the particular version of IEEE 1394 compatible with the claimed buses [e.g., 1394-1995, 1394a-2000, 1394b-2002]. Examiner submits that different versions inherently have different characteristics [e.g., system

requirements, performance] that would affect the scope of the claims. Prior art is still applied in the following rejections.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 6-7, 14-16, 19-21, 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamanaka et al., US Patent 4807259, hereinafter Yamanaka.

7. In re claim 1, Yamanaka discloses a method of synchronizing one or more devices on a first bus [associated with master; e.g., 10, 17] with one or more devices on a second bus [associated with slaves; e.g., 20, 27] [fig.3], the method comprising:

- Acquiring first bus timing information [e.g., TM] and second bus timing information [e.g., TS] from the first bus and the second bus respectively [col.7, ll.6-32; timing of components including devices and bus of each station refer to each respective clock].
- Determining a timing offset [TD] between the first bus and the second bus [col.7, ll.24-40].
- Broadcasting the timing offset to the one or more devices on the second bus so that the one or more devices on the second bus can adjust their timing to be synchronized with the one or more devices on the first bus [col.7, ll.34-49].

8. As to claim 2, Yamanaka discloses, wherein acquiring timing information from the first bus and the second bus comprises: taking a first time measurement [TM] for the first bus; taking

a time measurement [TS] for the second bus; and, taking a second time measurement [TDE] for the first bus [col.7, ll.6-25]; wherein the time measurement for the second bus is taken midway between the first and second time measurement for the first bus [TS taken between TM and TDE]; and wherein determining the timing offset comprises: calculating an average [TM + t1] of the first and second time measurements for the first bus; and subtracting the time measurement for the second bus from the average [col.7, l.40].

9. As to claims 6, 20, 23, Yamanaka discloses, wherein the one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on timing information of the first bus [col.1, ll.24-55; measurement at predetermined time in synch with master].

10. As to claims 7, 21, 24, Yamanaka discloses, wherein the one or more devices on the second bus adjust their timing by determining timing information of the first bus by applying the timing offset to the timing information of the second bus [col.7, ll.42-47].

11. As to claim 14, Yamanaka discloses, comprising respectively associating first [17] and second [27, 37] clocks with the first and second buses for generating timing information for the first and second buses.

12. As to claim 15, Yamanaka discloses, comprising automatically broadcasting timing information on the first and second buses [col.7, l.62 – col.8, l.2; automatically after adequate timing].

13. As to claim 16, Yamanaka discloses, wherein the method is carried out on a data processor [1] comprising first and second interfaces [part of 18] coupled to the first and second buses, respectively, and wherein acquiring timing information from the first bus and the second

bus comprises querying the first and second interfaces for the timing information [col.7, ll.6-25; 18 inherently uses some interface in the broadest interpretation to access master and slave times].

14. In re claim 19, Yamanaka discloses each and every limitation as discussed above in reference to claim 1 [i.e., separate master bus corresponds to the first bus of claim 1 and first and second buses corresponds to the second bus of claim 1].

15. In re claim 22, Yamanaka discloses each and every limitation as discussed above in reference to claims 1 and 16. Yamanaka discloses the apparatus [fig.3] comprising:

- A processing element [10] coupled to the first and second buses by the first and second interfaces respectively [e.g., 29, 39] to receive timing information for the first and second buses.
- A program memory coupled to the processing element, the program memory containing software instructions programmed to cause processing element to calculate a timing offset between the first bus and the second bus and broadcast the timing offset to the one or more devices on the second bus by means of the second interface [inherently, some memory is required to store the instructions in order for 10 to perform accordingly].

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 3-4, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claims 1, 2 above, and further in view of Baker, US Patent 6650719.

18. Yamanaka taught each and every limitation as discussed above. Yamanaka did not disclose calculating a drift rate of the timing offset.

19. In re claims 3 and 18, Baker discloses a method comprising calculating a drift rate of the timing offset and broadcasting the drift rate along with the timing offset [col.1, ll.12-49].

20. In re claim 4, Baker discloses, wherein calculating the drift rate comprises calculating a first order time derivative [col.1, ll.34-49].

21. In re claim 18, Yamanaka discloses, storing the timing offset [col.7, ll.42-47]; adjusting timing of the one or more devices on the second bus to be synchronized with the one or more devices on the first bus based on the broadcast timing offset and timing information of the second bus [col.1, ll.7-68]; and repeating synchronization steps [col.8, ll.3-19]. Baker discloses, if at least two timing offsets have been stored, calculating a drift rate based at least in part on a difference between two of the stored offsets and a time elapsed between when the two stored offsets were determined, otherwise setting the drift rate to zero [col.1, ll.34-49; derivative of zero coefficient would be zero].

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Baker before him at the time the invention was made, to modify the method taught by Yamanaka to include the drift rate calculation taught by Baker, as drift rates are well know in the art and suitable for use in the system of Yamanaka [digital transmission system]. One of ordinary skill in the art would have been motivated to make such a combination as it provides an important parameter in processing signals in a digital transmission system [Baker: col.1, ll.12-32].

23. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claim 1 above, and further in view of Yagita et al., US Patent 6081324, hereinafter Yagita, and Pennywitt et al., US Patent 6434562, hereinafter Pennywitt.

24. Yamanaka taught each and every limitation as discussed above. Yamanaka did not disclose using cameras in the industrial setting and the details of frame processing.

25. Yagita discloses the one or more devices that comprise a plurality of cameras [col.5, ll.31-57].

26. Pennywitt discloses the one or more devices adjust their timing by selectively reading an adjustable amount of extra data for each frame [col.17, ll.49-61].

27. It would have been obvious to one of ordinary skill in the art, having the teachings of Pennywitt, Yamanaka and Yagita before him at the time the invention was made, to modify the method taught by Yamanaka to include the monitoring cameras taught by Yagita and the frame teachings of Pennywitt, in order to obtain the claimed apparatus. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to monitor foreign materials in an industrial setting such as Yamanaka's [Yagita: col.5, ll.31-57] while properly synchronizing data rates of the camera images [Pennywitt: col.17, ll.49-61].

28. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claim 1 above, and further in view of Lisitsa et al., US Patent 6766407, hereinafter Lisitsa.

29. Yamanaka taught each and every limitation as discussed above. Yamanaka did not discuss the details of the bus.

30. Lisitsa discloses buses compliant with electronics standard IEEE 1394 [col.1, ll.59-65].

31. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Lisitsa before him at the time the invention was made, to modify the method taught by Yamanaka to include the IEEE 1394 taught by Baker, as IEEE 1394 is well know [prevalent] in the art and suitable for use in the system of Yamanaka [digital transmission system]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase data transfer speeds [Lisitsar: col.1, ll.59-65].

32. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claim 22 above.

33. Yamanaka discloses the apparatus wherein the first and second interfaces and the processing element are all located within a data processor [1] configured to process data received from the one or more devices on the first bus and the one or more devices on the second bus [fig.3a].

34. In re claim 25, Yamanaka did not disclose explicitly a bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses. Examiner hereby takes Official Notice that it is well known in the art to set the bandwidth of devices, particularly to set the bandwidth to the maximum allowable bandwidth of the bus used for communication, and that one with ordinary skill can setup the bandwidths so that a bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses.

35. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka before him at the time the invention was made, to setup the bandwidths so that a

bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses, as the setting of each device's bandwidth to the maximum possible for communication would result in a bandwidth of the one or more devices [e.g., cpu set to use communication bus fully] on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses [since cpu is set to maximum of the bus, additional bandwidth of any other device would exceed the maximum of the bus]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to allow each device to communicate at the maximum bandwidth.

36. In re claim 26, Yamanaka did not disclose explicitly the program memory is also located with the data processor. Examiner had taken Official Notice that it is well known in the art to have a program memory be located within some structure [data processor] along with the processing element.

37. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka before him at the time the invention was made, to have the program memory be located within the data processor, as it is extremely well known [most computer contains a program memory with associated processing element] and suitable for use with the system of Yamanaka. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to group essential elements in an area.

38. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claim 22 above, and further in view of Yagita et al., US Patent 6081324, hereinafter Yagita.

39. Yamanaka taught each and every limitation as discussed above. Yamanaka did not disclose using cameras in the industrial setting.

40. Yagita discloses the one or more devices that comprise a plurality of cameras, wherein all of the pluralities of cameras are positioned to encircle an image area and to record images of the image area [col.5, ll.31-57].

41. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Yagita before him at the time the invention was made, to modify the method taught by Yamanaka to include the monitoring cameras taught by Yagita, in order to obtain the claimed apparatus. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to monitor foreign materials in an industrial setting such as Yamanaka's [Yagita: col.5, ll.31-57].

42. Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claims 1, 19 and 22, respectively above, and further in view of Chaudhry et al., US Publication 20020152420, hereinafter Chaudhry.

43. Yamanaka taught each and every limitation as discussed above. Yamanaka did not disclose explicitly a plurality of processors [devices] within each slave station.

44. Chaudhry discloses simultaneously broadcasting the data value [timing offset] to a plurality of devices [redundant processors] on the second bus [170] [0017, 0020].

45. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Chaudhry before him at the time the invention was made, to modify the slave stations taught by Yamanaka to include the redundant processors taught by Chaudhry in order to obtain the claimed apparatus comprising simultaneously broadcasting the timing offset to a plurality of devices on the second bus [of the slave stations] and regulating a timing of each of the plurality of devices on the second bus based at least in part upon the timing offset. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to tolerate faults in processing systems [Chaudhry: 0016].

Response to Arguments

46. Applicant's arguments filed November 24, 2006 have been fully considered but they are not persuasive.

47. Applicant argues that "person of skill in the art would understand the method of averaging timing offsets... implicitly requires these time measurements to be performed at equally spaced-apart intervals". Examiner had not noted this point and submits that Applicant did not provide evidence of the alleged implicit requirement.

48. Applicant argues that "claim 12 is satisfied by compliance with *any* IEEE 1394 standard". Examiner points to Applicant's admission that "IEEE 1394 is currently define... for IEEE 1394-1995 (original version) and IEEE 1394a-2000 and 1394b-2002 (the amendments)" as evidence that the standard has different versions that give rise to different metes and bounds of a claim, rendering the claim indefinite.

49. Applicant's arguments with respect to Yamanaka are not persuasive in view of the new rejections above.

Conclusion

50. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
December 1, 2006

THUAN N. DU
PRIMARY EXAMINER